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Fully Patterned Low-Voltage Transparent Metal Oxide Transistors Deposited Solely by Chemical Spray Pyrolysis

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All-inorganic transparent thin-film transistors deposited solely by the solution processing method of spray pyrolysis are reported. Different precursor materials are employed to create conducting and semiconducting species of ZnO acting as electrodes and active channel material, respectively, as well as zirconium oxide as gate dielectric layer. Additionally, a simple stencil mask system provides sufficient resolution to realize the necessary geometric patterns. As a result, fully functional low-voltage n-type transistors with a mobility of 0.18 $cm^2V^{-1}s^{-1}$ can be demonstrated via a technique that bears the potential for upscaling. A detailed microscopic evaluation of the channel region by electron diffraction, high-resolution and analytical TEM confirms the layer stacking and provides detailed information on the chemical composition and nanocrystalline nature of the individual layers.

1. Introduction

Chemical spray pyrolysis (CSP) is a versatile solution-based technique, which offers the deposition of various high quality materials on large area substrates at moderate temperatures (typically 200–500 °C) and with comparatively inexpensive equipment.[1] Therefore, this technique is of great interest for low cost fabrication of devices such as thin-film transistors (TFTs)[2] or solar cells.[3] CSP involves the vaporization of a precursor solution and subsequent transport of the resulting mist to a heated substrate where it reacts to form films of the desired material. The scope of materials obtainable by CSP includes a wide range of oxides and chalcogenides such as ZnO,[4] TiO_2,[5] SnO_2,[6] Al_2O_3,[7] or CdSe.[8] Doping or ternary/quaternary systems can additionally be realized by a simple blending of different precursor solutions.[9–11] Using the CSP technique, the material requirements of thin films for all the basic components of electronic devices can be met, as semiconductors,[12] conductors (especially transparent conductive oxides),[13] as well as dielectrics[14] can be deposited. However, to create devices where all these individual materials act together, the ability for patterning and interface control is essential. While etching processes may be applied for that purpose, the choice of etchants suitable for selective etching may be difficult due to the chemical similarity between many oxide materials. Furthermore, the etching requires additional process steps, e.g., lithography, which causes the whole fabrication to be slower, less facile, and ultimately more expensive.

In this work, we use a simple stencil-mask approach to achieve direct patterning during the CSP process. We combine different materials and integrate them to form patterned and fully functional all solution-deposited thin-film transistors. The top-gated TFTs are composed of lithium-doped zinc oxide as semiconductor (ZnO:Li), indium-doped ZnO (ZnO:In, IZO) as conductive electrodes (source, drain, gate), and zirconium oxide as dielectric material. The semiconductor and dielectric material were selected because they already demonstrated excellent performance in TFT devices.[14] Furthermore, besides aluminum doped zinc oxide, IZO is one of the most promising transparent conductive oxides to replace the state-of-the-art material indium tin oxide.[15] All the materials feature large band gaps, which render them transparent in the visible spectrum. To the best of our knowledge, this is the first report on TFTs where all components were deposited and patterned using only the spray-pyrolysis technique.

2. Results and Discussion

Sufficient pressure to the stencil mask during the spray process is a key requirement to achieve acceptable patterning resolution. Otherwise, the vaporized precursor is allowed access to areas on the substrate that are supposed to be covered by the mask, resulting in undesired broadening of the patterns with undefined line edge roughness. In preliminary tests it was found that CSP patterns with a geometrical deviation in the range of 10% compared to the mask pattern could be realized for feature sizes above ≈100 µm using the clamping setup as shown in **Figure 1**a,b.

In order to qualify our approach, we discuss the properties of the materials individually, starting with the conducting electrodes used as source, drain and gate in the transistor. The conductivity of spray pyrolysis derived In-doped ZnO was investigated by two-point current-voltage measurements on CSP patterned dumb-bell shaped structures (length: 13 mm, width: 1 mm). A photograph and cross-sectional profile of

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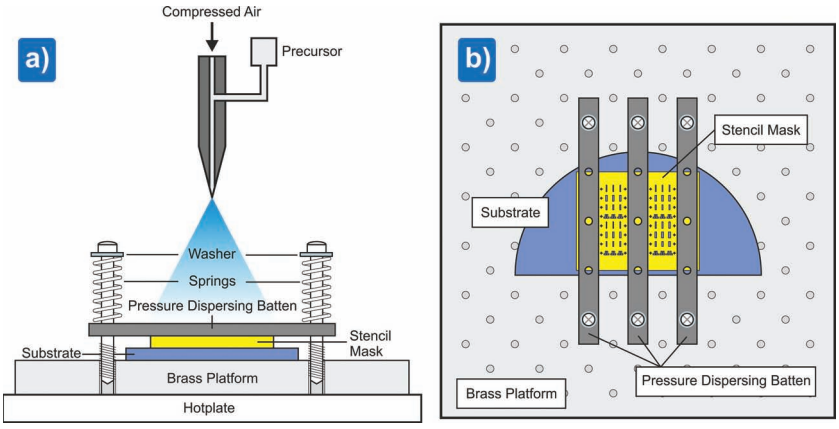

Figure 1. Schematic spray pyrolysis setup, including a) cross section and b) top view of the clamping mechanism used to fasten substrate and mask during the spray process.

such a structure are displayed in **Figure 2**a,b. On average, the film thickness in the inner region of the pattern is determined with approx. 100 nm. As evident from the height profile, the edges between ZnO and the substrate are not abrupt, but feature a rather gradual transition. The uneven height distribution is attributed to the manual operation of the spray gun and may be increased by shadow effects when the spray direction differs from a strict 90° incident angle towards the substrate and through the stencil mask.

The conductivity σ was calculated according to Equation 1:

$$\sigma = \frac{1}{AR} \quad (1)$$

with length l, area A and resistance R. The area was determined by integration over the respective cross-sectional profile.

Undoped ZnO exhibits a low conductivity of about 10^{-5} S cm^{-1}, which drastically increases to 10^{-1} S cm^{-1} for the In-doped sample. Indium doping relies on the substitution of Zn^{2+} ions with In^{3+} ions,[16] releasing an additional electron as charge carrier. The conductivity value for the In-doped ZnO is still below those of 10^{2}–10^{3} S cm^{-1} reported for other CSP deposited IZO layers in the literature.[17–19] However, those values were obtained for higher deposition temperatures, considerably thicker IZO layers (up to 1900 nm[20]), and/or different indium sources which all can be favorable for increased σ. To further increase the conductivity we applied a hydrogen plasma treatment to the ZnO and IZO samples.

It was proposed that hydrogen in ZnO forms a complex, involving one H atom coordinated by four Zn atoms, which acts as shallow donor.[21] Plasma treatments or annealing in hydrogen-rich environments have been demonstrated to increase the conductivity of ZnO, especially in systems with high surface-to-volume ratio such as thin films and nanowires.[10,22,23]

In our samples, the conductivity after H_2 plasma exposure was increased up to values of 42 and 89 S cm^{-1} for undoped ZnO and IZO, respectively, placing both within the same order of magnitude. However, the stability of the hydrogen treatment strongly depends on the indium doping. For the undoped ZnO sample the beneficial impact of the H_2 plasma exposure on σ decreases over time, indicated by a factor 20 drop in conductivity over the course of 16 days (cf. Figure 2c). In contrast, the plasma-treated

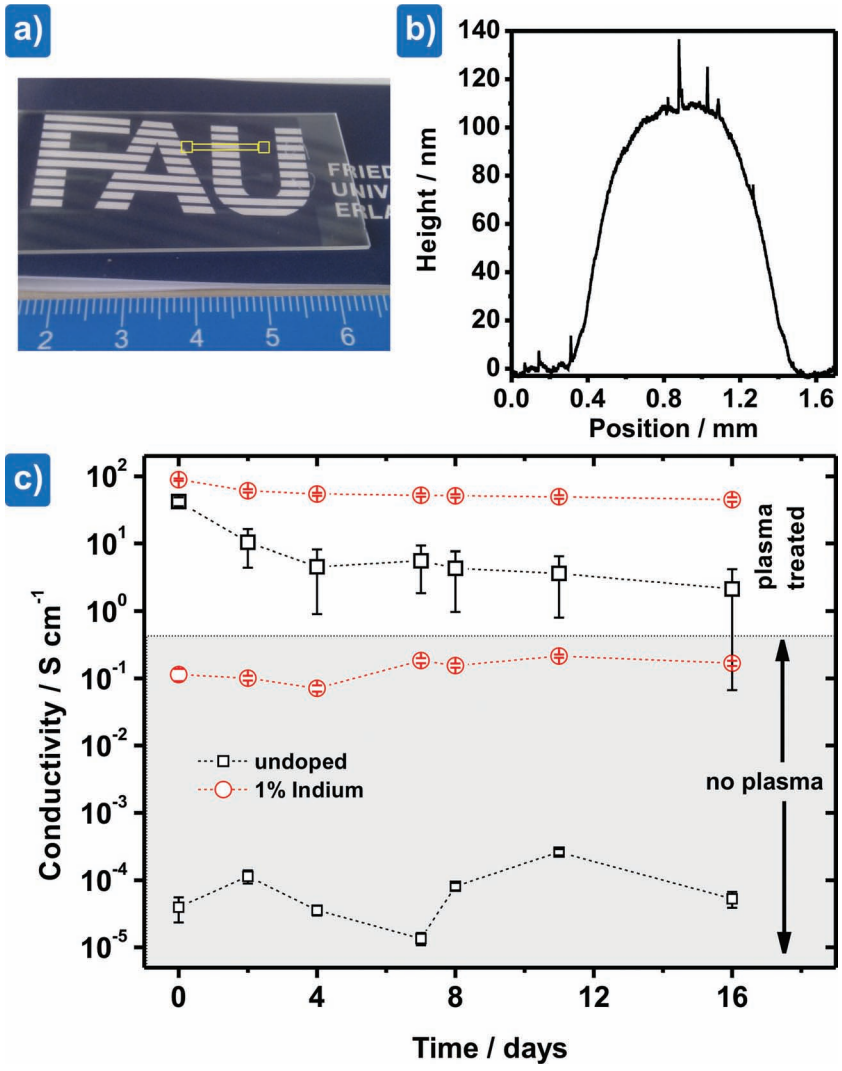

Figure 2. a) Transparent IZO dumbbell structures on glass substrate, one of which is highlighted in yellow to guide the eye. b) Cross-sectional height profile of dumbbell shaped ZnO patterns for conductivity measurements of In-doped ZnO. c) Progression of conductivity over time for undoped ZnO and IZO structures with and without hydrogen plasma treatment.

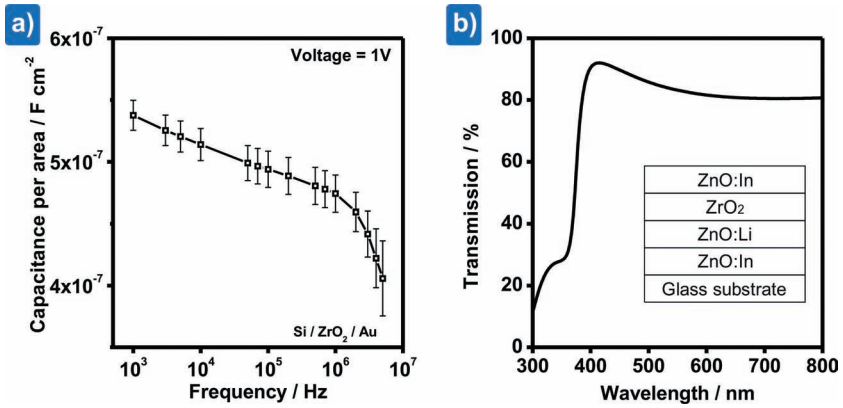

Figure 3. a) Capacitance-frequency plot for the dielectric zirconium oxide layer. b) Transmission of the complete stack with all deposited layers.

IZO sample remains virtually unaffected (σ only decreases by a factor of 2). The non-plasma-treated samples remain close to their initial conductivity values but feature a certain amount of fluctuation, which is attributed to common variations of the ambient atmosphere (Figure 2c).

The dielectric properties of the zirconium oxide layer were characterized in stacked capacitor devices featuring a highly doped Si wafer as back electrode and Au top contacts. High values in the order of several hundreds of nF cm^{-2} were determined for the area normalized capacitance C_A (**Figure 3**a) related to the frequency. For mobility calculations of the finished TFTs, the capacitance of 538 nF cm^{-2} at the lowest frequency of 1 kHz was used. Considering a dielectric permittivity $\varepsilon_{(ZrOx)} = 14$ (as reported for CSP derived zirconium oxide),[14] the vacuum permittivity ε_0, and Equation 2:

$$C_A = \frac{C}{A} = \frac{\varepsilon_0 \varepsilon(z_r o_x)}{d} \quad (2)$$

the layer thickness d results in 23 nm.

The optical characteristics were investigated on a glass slide that was coated, in parallel to the TFT fabrication, with a layer stack of each material. Figure 3b shows the transmission spectrum of the entire stack. We obtained promising transparency with values over 80% in the complete visible spectrum, qualifying our approach for possible applications in transparent electronics.

The complete process flow of the TFT fabrication is schematically summarized in **Figure 4**a. To realize the selected top-gate device structure, the IZO source and drain electrodes are deposited first (step 1), using the direct patterning during the CSP process. Subsequently, they are exposed to a H_2 plasma treatment to increase their conductivity (step 2). This is followed by the likewise patterned deposition of Li-doped Zno as semiconductor (3). Lithium was used as dopant here as it is known to increase the mobility in ZnO TFTs.[9,24] Next, zirconium oxide as dielectric material is applied without patterning over the complete substrate area (4), before the device is completed by deposition and H_2 plasma exposure of the IZO gate electrode (5,6). Besides the role as dielectric material in the device, the zirconium oxide additionally acts as a shielding barrier against unwanted hydrogen exposure of the semiconducting layer. An optical micrograph of a final device is shown in Figure 4b. The measured channel width W and length L are around 1400 and 140 µm, respectively, and thus featured less than 10% deviation from the nominal values of 1500 and 150 µm on the stencil mask. Especially the latter value is close to the lower end of structural dimensions which can still be reliably deposited with the

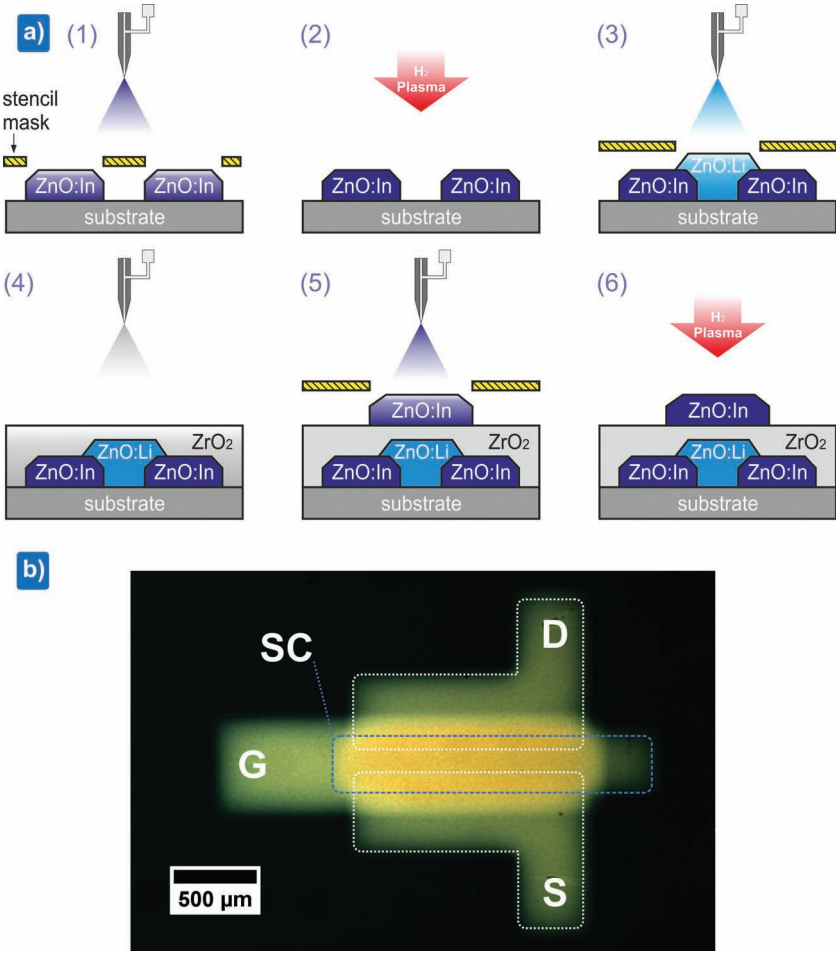

Figure 4. a) Schematic process flow of device fabrication. b) Light- optical micrograph of finished CSP derived transistor. The gate, source, and drain electrodes as well as the semiconductor pad are marked with G, S, D, and SC, respectively and partially framed to guide the eye. Please note that the color histogram was adjusted to achieve maximum contrast.

current setup (~100 µm). However, we note that a refined mask design and fabrication (i.e., thinner material) may very well lead to a higher achievable resolution. For instance, thin high resolution silicon stencil masks allow the deposition of metal structures by physical vapor deposition with channel length smaller 5 µm[25] and should be applicable for our CSP approach as well.

The expected stacking sequence within the central channel region between source and drain electrodes (ZnO:Li/ZrO_2/ZnO:In) is verified by TEM. All three sublayers are clearly distinguishable by HAADF-STEM and HRTEM imaging (**Figure 5**a–c), showing an excellent adhesion on the substrate. The measured thickness of each sublayer is around 20 nm. For the unpatterned zirconium oxide, this is in good agreement with the value calculated from the capacitance measurements. However, both patterned ZnO layers were expected to be considerably thicker (up to 100 nm). This mismatch is therefore attributed to increasing shadowing effects for decreasing feature sizes on the stencil mask. The initial roughness, which evolved due to the crystallization of the first deposited layer in the channel area (ZnO:Li), propagates through the zirconia and is reflected in the final surface topography of the device. Nevertheless, especially the interface semiconductor/dielectric (ZnO:Li/ZrO_2) is of excellent quality. This is of considerable importance for the final TFT device as that region represents the main pathway for electron transport along the active channel and its quality is essential for a good device performance.

It turned out that the ZnO:Li and ZnO:In layers are composed of dense crystallites with sizes of the order of the layer thickness (around 20 nm). The crystallites of the zirconium oxide layer possess similar sizes, as revealed by the HRTEM image Figure 5c, but exhibit a fine porosity (slightly darker nm-scaled regions in the central part of Figure 5b) even embedded within the crystalline structure of single ZrO_2 grains (cf. Figure 5b,c).

In order to evaluate the crystal phases of the nanocrystalline ZnO and ZrO_2 layers in the channel region selected area electron diffraction (SAED) patterns of the layer stack have been taken in cross-section geometry. The ring diffraction pattern shown in Figure 5d is obtained by averaging 12 individual SAED patterns from adjacent interface regions covering a total interface lengths of ~3 µm. In this way a reasonable statistics for a sound interpretation and further evaluation of the pattern is obtained. First, there is no indication for film texture which would be reflected in an uneven distribution of diffraction intensities along the ring perimeters. Secondly, by rotational averaging of the ring pattern (and subsequent background subtraction) a smooth radial intensity distribution profile, similar to a θ-2θ plot in XRD, can be obtained (Figure 5d, right side). All the peaks of the profile can be indexed by lattice planes of either hexagonal ZnO (red tics) or cubic/tetragonal ZrO_2 (blue tics) indicating that these two crystallographic phases preferentially form during the CSP process. Due to the pronounced peak broadening which results from the small crystallite sizes it is not possible to discriminate between cubic and tetragonal ZrO_2.[26] However, the formation of monoclinic ZrO_2 can be clearly excluded showing that cubic/tetragonal ZrO_2 is stabilized in the nanocrystalline film.[27]

The difference in average atomic number between ZnO and zirconia (+20%) is reflected in the HAADF-STEM images in Figure 5a,b), where the zirconium oxide appears slightly brighter (at least at the interface ZnO:Li/ZrO_2). In order to

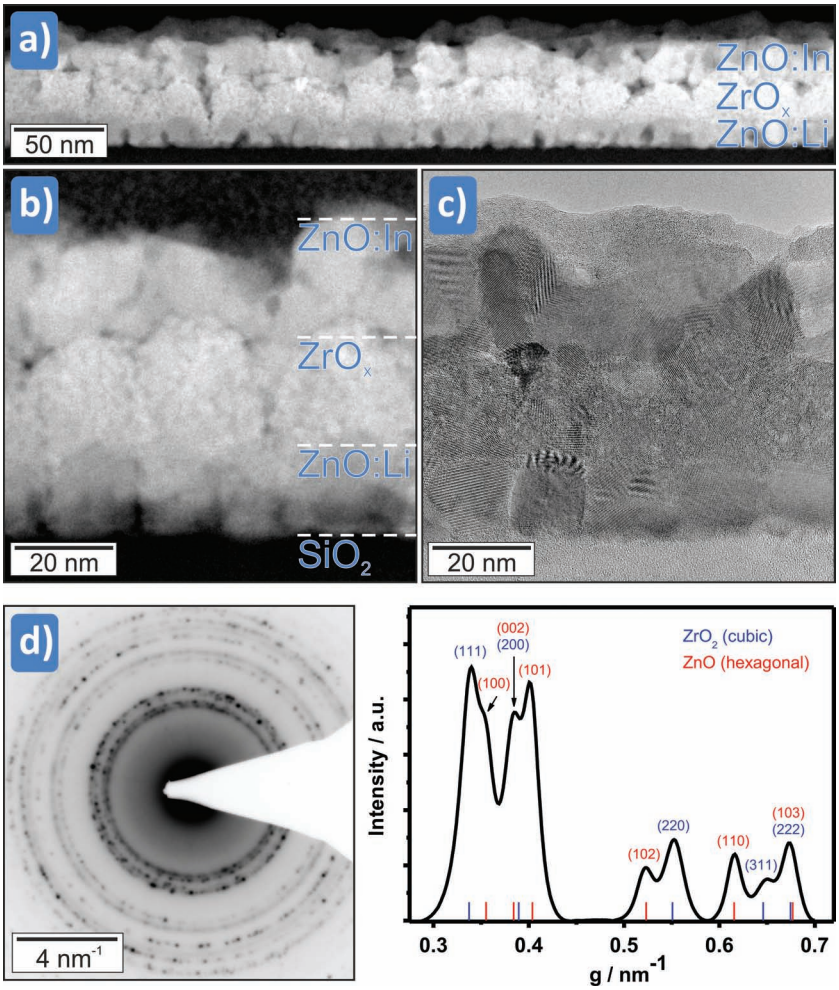

Figure 5. a) and b) HAADF-STEM images of cross section of TFT (all CSP-derived layers are distinguishable as indicated) in the channel region (SiO_2 below). c) HRTEM micrograph of similar region (same magnification as (b)) showing the excellent crystallinity of the derived layers. d) SAED pattern of the cross section including all three layers (contrast inverted for better visibility). In spite the small selected-area aperture size corresponding to ~250 nm on the sample a decent statistics (homogeneity of the rings of reflections in d) was achieved by averaging 12 individual patterns recorded from adjacent regions along the interface. The corresponding background subtracted radial intensity distribution profile is shown on the right-hand side. The apparent rings of reflections correspond to those expected from hexagonal ZnO and cubic (or tetragonal) ZrO_2 as indicated (see text).

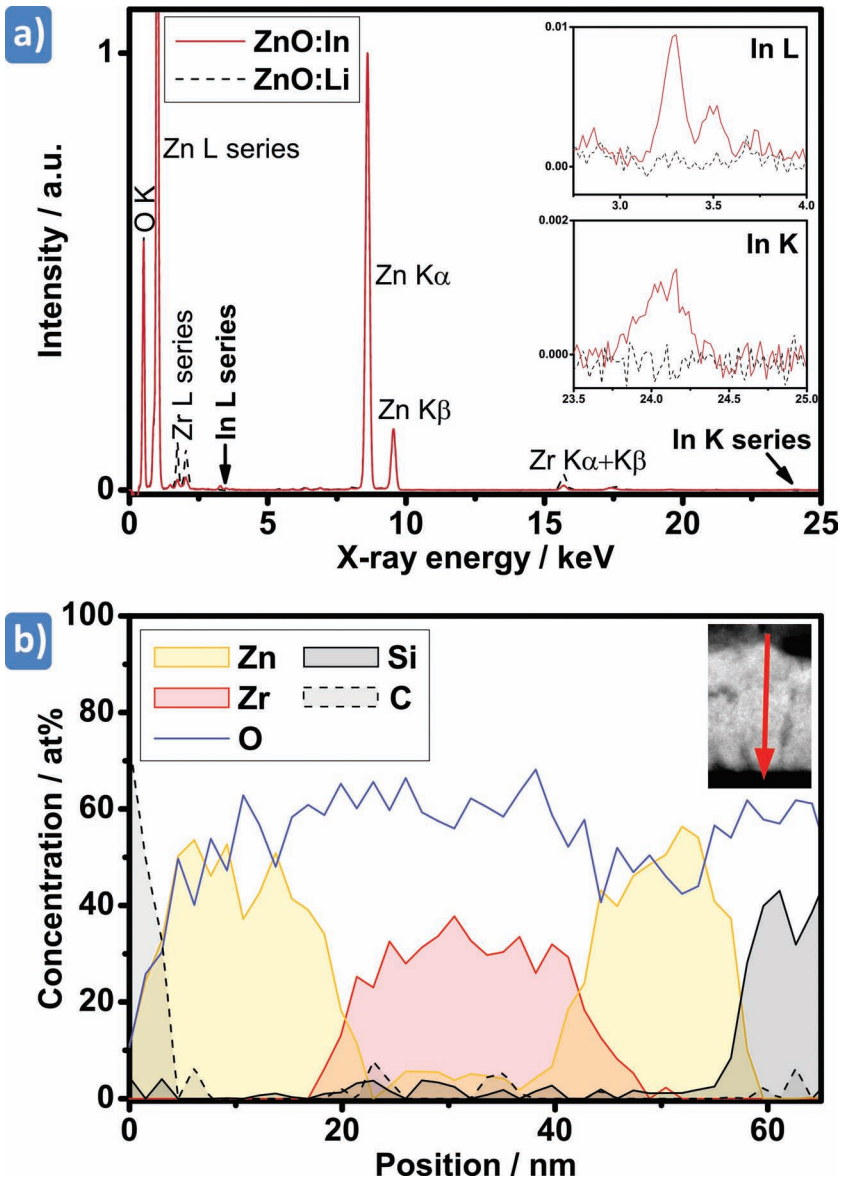

Figure 6. a) Representative EDXS spectra of ZnO:Li and ZnO:In (Zn Kα peak intensity ~5×10^4, both normalized respectively) showing the In-doping in the gate electrode. The measured In signal corresponds to 0.6 at% In on the cationic sublattice as derived from the quantification using theoretical ionization cross-sections. b) Quantified STEM-EDXS line scan (50 measuring points every 1.5 nm) across the stack as indicated in the inset (red arrow). The chemical variations of the order of around 15% are due to the statistics of the measurement. The limited resistance against severe electron-beam damage even under moderate illumination impeded measurements with much better count rates.

proof the stacking sequence chemically and thus to verify the location in the TFT channel, EDXS measurements of the semiconductor (ZnO:Li) and the gate electrode (ZnO:In) were conducted (**Figure 6**a). Next to the most pronounced peaks of Zn and O, both representative spectra (normalized with respect to the Zn Kα peak) show negligible signal contributions attributed to the interjacent zirconium oxide layer, which may result from stray electrons and beam broadening. The intensity contributions due to the dissolved dopant in the gate-electrode layer (In K and In L emission lines, respectively) are barely visible. Therefore, both relevant energetic regions are depicted in the insets. In spite of the low In concentration in the gate electrode, the element is clearly detected (cf. spectra/insets in Figure 6a). The In concentration, quantitatively determined using theoretical cross-sections, arises to be around 0.6 at% on the cationic sublattice ($c_{Zn}/c_O \approx 50$ at%/50 at%), which is slightly smaller than the expected value of 1 at% from the precursor concentration. Complementary to HAADF-STEM imaging, EDXS line scans (Figure 6b) across the layers (indicated in the inset) confirm the excellent chemical separation of the three layers. The expected compositions (ZnO, ZrO_2, SiO_2) regarding the main elements in the layers are reflected in the quantitative elemental distributions in Figure 6b. The coarse variations are due to statistical errors, which are of the order of 10% for each element, arising from the low count rates of the measurement. Better statistics could not be achieved because of the limited stability of the oxide layers in the cross-section sample under the electron beam even at moderate illumination (e.g., in comparison to similar thin films processed at much higher temperatures). This might be due to incomplete pyrolysis of the precursor leading to carbonaceous residuals (Figure 6b). The Li dopant in the semiconductor could not yet be detected, neither by EDXS (principle problem of X-ray yield) nor electron energy-loss spectroscopy (EELS), which is in general well-suited to measure the Li-K ionization edge at an energy loss of 55 eV. The reliable separation of the weak element-specific signal (trace of Li) and the background was impeded by the not accurately known shape of the plasmon-near background in the EEL spectra.

Successful device operation of the completed TFT is demonstrated in the transfer and output characteristics in **Figure 7**a and b. The devices exhibit typical n-type transistor behavior in enhancement mode with a good current saturation. The transfer characteristics exhibit a small hysteresis of ~800 mV. In accordance to the limited stability during TEM investigations, we dedicate this to residuals of carbon species in the layers due to a partially incomplete precursor conversion during the fabrication at only moderate temperatures. These residuals are believed to cause trapping/detrapping of charge carriers during the gate voltage sweep and thus initiate the hysteresis. Since both source/drain electrodes and semiconductor are comprised of ZnO the expected injection barrier is low and consequently no indications of significant contact resistance are obtained in the output curve. Low-voltage operation is ensured by the high capacitance of the zirconium oxide dielectric layer. The threshold voltage and

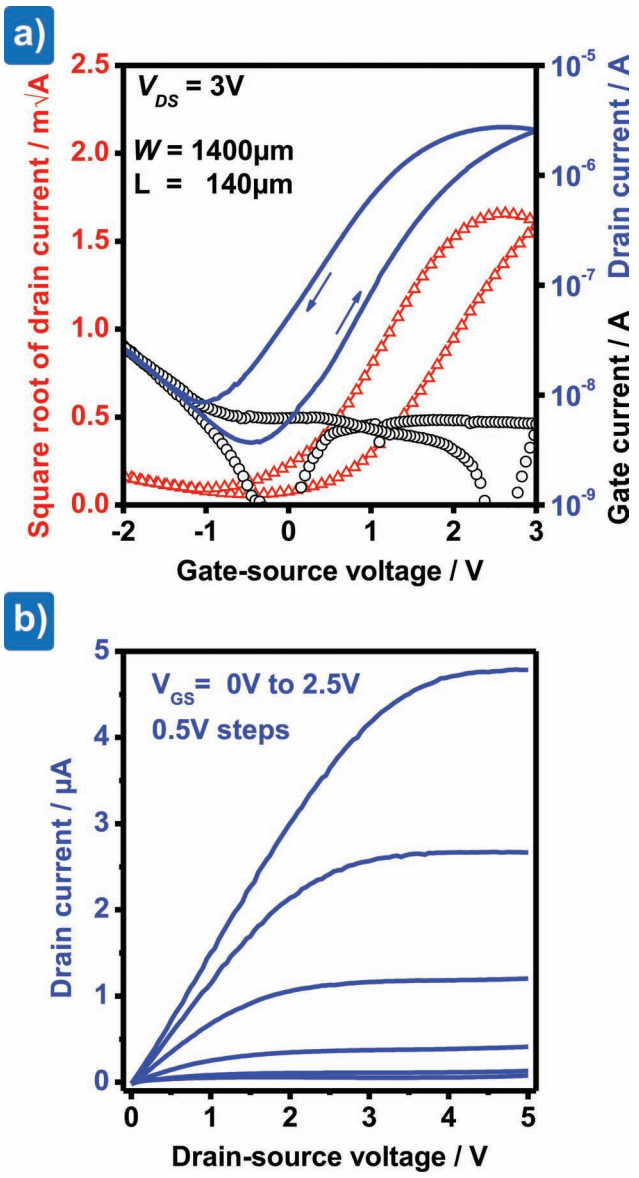

Figure 7. a) Transfer characteristic of all CSP deposited TFT, (solid blue line: drain current, black circles: gate current, red triangles: square root of drain current). b) Corresponding output characteristics.

on/off ratio were determined to be 0.66 V and 6×10^2, respectively. Electron mobilities in the range of 10^{-1}–10^{-2} cm^2 V^{-1} s^{-1} were obtained with a maximum value of 0.18 cm^2 V^{-1} s^{-1}. Significantly higher mobilities (between ≈15–85 cm^2 V^{-1} s^{-1}) were already achieved with the spray pyrolysis method and similar materials systems for semiconductor and dielectric,[2,9,12,14] albeit using Al source and drain contacts instead. With a conductivity value of 89 S cm^{-1} for the IZO electrodes in this work, there is still a difference of ≈4 orders of magnitude compared to commonly employed metal electrodes. The current transport within the electrodes must therefore be considered a prominent limitation for device performance and consequently subject to further improvements. Further limiting factors can be seen in the propagation of roughness throughout each additional layer as well as the moderate process temperatures. For deposition temperatures above 400 °C, especially the pyrolysis of the ZrO_2 precursor is expected to be more complete, thus leading to reduced carbon contents in the films and consequently a reduced hysteresis in the device characteristics. However, the presented results already offer a potential route for the fabrication of low-cost and large area fabrication of entire electronic devices.

3. Conclusions

In order to prepare transparent inorganic TFTs a comparatively simple and cost-effective approach is presented that is completely based on CSP deposition. To realize the high transmissivity of the final devices in the optical regime (>80%), Li-doped ZnO (semiconductor), hydrogen-plasma treated In-doped ZnO (all electrodes), and ZrO_2 (dielectric) were utilized. All components of the TFTs were patterned simply by using a stainless steel stencil mask. Furthermore, the presented process is well-suited to prepare the different components and thus the final device with well-defined microstructure and properties at a moderate temperature of 400 °C. The final TFTs exhibit low-voltage operation and electron mobilities up to 0.18 cm^2 V^{-1} s^{-1}, thus providing evidence for the capabilities of the CSP technique.

4. Experimental Section

Precursor Preparation: All precursor formulations were created with methanol as solvent. The precursor for the semiconductor deposition was composed of 0.3 M zinc acetate dihydrate with addition of lithium acetate to adjust a cationic Li dopant concentration of 1 at%. The conducting IZO electrodes were realized from a 0.3 M zinc acetate dihydrate solution with addition of indium nitrate to realize an In dopant concentration of 1 at%. Zirconium acetyl acetonate with a concentration of 0.2 M was employed as precursor material for the deposition of the dielectric zirconium oxide layer.

Spray Pyrolysis Deposition: In all CSP processes, the substrate temperature was set to 400 °C. The spraying was performed with a manually operated airbrush gun at a vertical distance of 20–30 cm. The spray rate was approx. 2–3 mL min^{-1} using compressed air as carrier gas. Patterned deposition with the CSP process was achieved by spraying through a laser cut stainless steel stencil mask (thickness 0.3 mm) that was firmly pressed against the substrate. Pressure was applied via three brass battens that were pushed down by means of several springs. The schematical setup of the process and the custom-built brass platform including the clamping system is shown in Figure 1.

Device Fabrication: ZnO and IZO patterns were deposited in dumb-bell shape in order to investigate their conductivity by two point current-voltage measurements. A 3 min hydrogen plasma treatment was applied to some of these dumb-bell structures, using a plasma chamber (Pico, Diener electronic GmbH, Germany) with 200 W at pressure of 0.2 mbar pressure.

The fabrication of CSP derived top-gated TFTs followed the procedure outlined in Figure 4a. Patterned IZO source and drain electrodes were first deposited using the stencil mask and clamping system and afterwards exposed to H_2 plasma to increase their conductivity. Next, following the manual alignment of the stencil mask, the ZnO:Li semiconductor pattern was fabricated. Afterwards, the zirconium oxide was deposited as dielectric material over the whole area.

Characterization: A Tencor Alpha Step D-100 profilometer was used to obtain information onheight profiles across the dumb-bell structures used in the conductivity experiments. Transmission measurements were performed with a Varian cary 6000i UV-vis-NIR spectrophotometer. The electrical characterization was carried out in ambient atmosphere using an agilent B1500A parameter analyzer. The microstructure and chemistry of the final TFT stack below the gate electrode (stack sequence: semiconducting ZnO:Li/ZrO_2/ conducting ZnO:In) was characterized in detail by means of transmission electron microscopy (TEM) by high-resolution TEM, atomic-number contrast scanning TEM (high-angle annular dark-field STEM, HAADF STEM), and energy-dispersive X-ray spectroscopy (EDXS). Therefore, cross-sectional TEM samples were prepared in wedge-shaped geometry (including grinding, tripod polishing, Ar-ion milling at 2.5 kV) after site-specific extraction of the relevant region by cutting. For this study, our image-side aberration-corrected Titan^3 80–300 microscope was operated at 200 kV in order to minimize electron-beam induced damage of the sample.

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